Patent Claims

1. A data processing method using a multiplicity of processors (P1-P5) which operate in parallel and to which a respective command (CMP1, CMP2, MOV1, MOV2, FSEL) for data processing is supplied simultaneously, at least one of the processors (P5) being alternatively supplied with a program flow control command or a condition command (FSEL), the supplying of the condition command (FSEL) deactivating the parallel execution of a further command (CMP1, CMP2, MOV1, MOV2) in at least one of the further processors (P1-P4).

2. The data processing method as claimed in claim 1, wherein the supplying of the condition command (FSEL) has the effect that the computational result of one of the processors (P1, P2) is not written back into a target register (RF) which is provided.

3. The data processing method as claimed in claim 1 or 2, wherein the supplying of the condition command (FSEL) has the effect that an address is not calculated.

4. The data processing method as claimed in claim 1, 2 or 3, wherein the supplying of the condition command (FSEL) has the effect that a command is not executed by the at least one of the further processors (P1-P4).

5. The data processing method as claimed in one of the preceding claims, wherein the further commands (CMP1, CMP2, MOV1, MOV2) comprise arithmetic computational commands and/or move commands.

6. The data processing method as claimed in one of the preceding claims, wherein the condition which

is associated with the condition command (FSEL) is the same for all the further processors (P1-P4).

7. The data processing method as claimed in one of the preceding claims, wherein the condition which is associated with the condition command (FSEL) is different for all the further processors (P1-P4).